In the Claims:

1. (currently amended) A semiconductor device comprising:

a semiconductor chip having a planar active surface including an integrated circuit, said integrated circuit having metallization patterns including a plurality of contact pads at said planar active surface;

a protective overcoat over said planar active surface, said protective overcoat including windows exposing said plurality of contact pads, said windows having sidewalls;

an added conductive layer covering each of said contact pads, said window sidewalls, and a portion of said protective overcoat surrounding said windows, said added layer having a surface conforming to said contact pads, said window sidewalls, and said portion of said protective overcoat adjacent said chip and a planar outer surface.

2. (previously presented) The device according to Claim 1 wherein said chip metallization is aluminum, copper, or alloys thereof.

3. (previously presented) The device according to Claim 1 wherein said conductive layer consists of at least two conductive sub-layers, one being a conductive diffusion barrier, the other, outer layer being bondable.

4. (previously presented) The device according to Claim 3 wherein said conductive diffusion barrier is selected from a group consisting of nickel, vanadium, titanium, tungsten, tantalum, osmium, chromium, and aluminum.

5. (previously presented) The device according to Claim 3 wherein said bondable layer is selected from a group consisting of gold, palladium, platinum, silver, and alloys thereof.

6. (currently amended) The device ~~package~~ according to Claim 1 wherein said outer surface has a flatness suitable for metal interdiffusion with another flat surface formed by a metal suitable for interdiffusion.

7. (previously presented) The device according to Claim 1 further comprising:

a distribution of said contact pads such that an area portion of said active chip surface is available for attaching a thermally conductive plate, said plate having a thickness compatible with the thickness of said conductive pad layer.

8. (previously presented) The device according to Claim 7 wherein said plate has an outer surface suitable for metallurgical bonds.

9. (previously presented) The device according to Claim 8 wherein said plate surface is solderable.

10. (previously presented) The device according to Claim 7 wherein said contact pads are arrayed along the periphery of said chip and said plate is located inside said periphery.

11. (previously presented) The device according to Claim 7 wherein said contact pads are arrayed in the center of said chip and said plate is formed as a frame around said contact pads.

12. (previously presented) The device according to Claim 1 wherein said semiconductor chip is made from a material selected from a group consisting of silicon, silicon germanium, gallium arsenide, and any other semiconductor material used in integrated circuit fabrication.

13. (previously presented) The device according to Claim 1 further comprising encapsulation material protecting at least the chip surface opposite said active surface.

14. (previously presented) The device according to Claim 13 wherein said encapsulation material is a molding compound.

15. (previously presented) The device according to Claim 1 further comprising a metallic or insulating substrate adjacent said planar active surface of said chip, said substrate having terminal pads aligned with the distribution of said chip contact pads, each terminal pad being bonded to one of said chip contact pads having said added layer, respectively, such that electrical contact between said chip and said substrate is established, while forming a gap therebetween having a width of approximately said added layer thickness.

16. (previously presented) The bonding according to Claim 15 wherein said bonding is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

17. (previously presented) The device according to Claim 15 further comprising encapsulation material protecting at least the chip surface opposite said active surface and filling said gaps.

18. (previously presented) The device according to Claim 17 further comprising a substrate addition suitable for attaching said device to a board, said addition selected from a group consisting of solder balls, conductive lands, and bondable surface finish.

19. (previously presented) The device according to Claim 1 further comprising a protective layer on the chip surface opposite said active surface, said protective layer shielding against light and disturbing environmental influences.

20. (previously presented) The device according to Claim 19 wherein said protective layer comprises hardened polymeric material.

21. (previously presented) A semiconductor assembly comprising:

a semiconductor chip having a planar active surface including an integrated circuit, said circuit having metallization patterns including a plurality of contact pads at said planar active surface, a protective overcoat over said planar active surface, said protective overcoat including windows exposing said plurality of contact pads, each of said contact pads having an added conductive layer covering each of said contact pads, said window sidewalls, and a portion of said protective overcoat surrounding said windows, said added layer having a surface confroming to said contact pads, said window sidewalls, and said portion of said protective overcoat adjacent said chip and a planar outer surface; and

an assembly board having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said chip contact pads;

said chip metallurgically bonded to said board so that each of said chip contact pads is connected to a corresponding board terminal pad.

22. (previously presented) The assembly according to Claim 21 wherein said assembly board is selected from a group consisting of organic materials, including FR-4, FR-5, and BT resin, with or without strengthening or thermally modulating fibers; metals; and ceramics.

23. (previously presented) The assembly according to Claim 21 wherein said board terminal pads comprise an outer surface selected from a group consisting of gold, palladium, silver, platinum and alloys thereof.

24. (previously presented) The assembly according to Claim 21 wherein said metallurgical bonding of said outer layer surface of said contact pads to said terminal pads is selected from a group of techniques and materials comprising:

direct welding by metallic interdiffusion;

attachment by solder paste; and

attachment by conductive adhesive.

25. (previously presented) A semiconuctor assembly comprising:

a semiconductor chip having a planar active surface including an integrated circuit, said circuit having metallization patterns including a plurality of contact pads at said planar active surface, a protective overcoat over said planar active surface, said protective overcoat including windows exposing asaid plurality of contact pads, said contact pads distributed such that an area portio of said chip surace is available for attaching a thermally conductive plate;

each of said contact pads having an added conductive layer on said metallization, said added layer having a surface covering each of said contact pads, said window sidewalls, and a portion of said protective overcoat surrounding said windows adjacent said chip and a planar outer surface;

said thermally conductive plate, attached to said active chip surface, having a thickness compatible with the thickness of said chip contact layers, and a surface sutiable ofr metallurgical bonds; and

an assembly board adjacent said planar active surface of said chip having a plurality of planar, metallurgically bondable terminal pads in a distribution aligned with the distribution of said chip contact pads, and further having a thermally conductive site with a metallurgically bondable surface in a location aligned with the location of said chip plate;

said chip metallurgically bonded to said board so that each of said chiop contact pads is connected to the corresponding board terminal pad; and said plate is connected to said corresponding thermally conductive site.

26-32 (canceled)